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APUs and Processor Advancements for Embedded Applications

By Kelly Gillilan, Marketing Manager, AMD Embedded Solutions

t the beginning of a new year, it's interesting to look back at the technical advancements that have occurred in the prior 12 months.

Take AMD's Embedded Accelerated Processing Units (APUs) for example. In the past year we launched the highperformance AMD Embedded R-Series APU platform consisting of quad- and dual-core models running at 2.3 GHz (3.2 GHz boost) with AMD Radeon[™] 7000 series integrated graphics providing more than 570 GFLOPS of performance in just a 35 W TDP. Shortly after the launch of the AMD R-Series APUs, we released a new addition to our low-power AMD Embedded G-Series APU line-the 4.5 W TDP AMD T-16R APU for power-sensitive applications requiring efficient performance and high-definition graphics. These two families of APUs service different market segments, but both provide the unique combination of a powerful, yet power-efficient CPU with a discreet-level, high-performance GPU for a heterogeneous system architecture.

So how did we get here? We've seen CPUs transition from single-core architectures, where performance boosts typically were accomplished by increasing clock speed, to multi-core architectures able to handle multi-threaded applications efficiently. However, there are limits to how many cores a design can incorporate before the throughput performance levels off—that's because of the increase in "overhead" to manage such an architecture. GPUs also have undergone a significant transformation—from simply driving a display to driver-based programs to system-based programming models with power efficiency enhancements.

The next phase in processor evolution is currently unfolding. AMD's APUs combine multiple x86 CPU cores to handle serialized data with dozens or even hundreds of compute units in the GPU. These cores process parallelized data to provide a heterogeneous system architecture with excellent performance potential in low-power bands.

What does this mean for embedded applications? Over the past year I have seen our partners develop hardware solutions in very small form factors (such as Qseven) that are able to drive two full-HD independent displays from a fanless, compact enclosure. Systems like these are ideal for powering industrial control and factory automation systems as the industry phases out old arrays of buttons, knobs, and switches in favor of touch-panel controls with 3D manipu-



Kelly Gillilan Marketing Manager, AMD Embedded Solutions

Kelly Gillilan has worked extensively in embedded applications for most of the past decade. He currently is the Product Marketing Manager for the AMD Embedded Solution division, overseeing worldwide marketing strategy and activities. He holds a degree in Computer Engineering and is fluent in Mandarin Chinese.

lation. Some of our partners have combined the AMD R-Series APU-which supports four independent displays with the AMD Radeon[™] E6760 embedded discrete GPU-which supports six independent displays—to create systems capable of driving a total of 10 independent displays. These types of systems are ideal solutions for applications such as casino gaming and digital signage, where multimedia content must be large, bold, and eye-catching. Metrics for these systems also can be efficiently processed by using programming languages such as OpenCL[™] that compile specifically for heterogeneous system designs such as those based on AMD's APUs.

I can't predict the future, but one thing is certain: as these technologies continue to evolve and new innovations are introduced, embedded system designers and integrators will capitalize on new application and market opportunities that can lead to increased revenue streams. AMD MEEDDED

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Model	x86 Core Clock Speed Base/Boost	L2 Cache	GPU	DDR3 Speed	x86 Cores	UVD ¹ 3	AMD-V™ Tech. ²	EVP ³	Package	Max TDP
AMD Embedded R-Series APU – FS1r2 PGA										
R-464L	2.3/3.2 GHz	2MB x 2	AMD Radeon™ HD 7660G	DDR3-1600	4	Yes	Yes	Yes	FS1r2 (722-PGA)	35W
R-460H	1.9/2.8 GHz		AMD Radeon™ HD 7640G							
R-272F	2.7/3.2 GHz	4 MD	AMD Radeon™ HD 7520G		2					
R-268D	2.5/3.0 GHz	TIMB	AMD Radeon™ HD 7420G							
AMD Embedded R-Series APU – FP2 BGA										
R-460L	2.0/2.8 GHz	2 MB x 2	AMD Radeon™ HD 7620G	DDR3-1600	4	Vaa	Yes	Yes	FP2 (827-BGA)	25W
R-452L	1.6/2.4 GHz		AMD Radeon™ HD 7600G							19W
R-260H	2.1/2.6 GHz	2 MB	AMD Radeon™ HD 7500G		2	Tes				17\\/
R-252F	1.7/2.3 GHz	1 MB	AMD Radeon™ HD 7400G		2					17.00

1. Unified Video Decoder (UVD 3) for hardware decode of high definition video.

2. AMD Virtualization™ technology. When used as part of a DAS 1.0 implementation can improve the performance, reliability and security of embedded applications.

3. As part of a comprehensive security program, AMD strongly recommends enabling Enhanced Virus Protection (EVP) and using up-to-date thirdparty anti-virus software.

Note: Always refer to the processor/chipset data sheets for technical specifications. Feature information in this document is provided for reference only.





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AMD

OpenCL[™] Programming for Heterogeneous Computing Systems: Parallel Processing Made Faster and Easier Than Ever

By Todd Roberts, Software Manager, Embedded Solutions, AMD

arallel processing isn't really new. It has been around in one form or another since the early days of computing. As traditional CPUs have become multi-core parallel processors, with many cores in a socket, it has become more important for developers to embrace parallel processing architectures as a means to realize significant system performance improvements by taking advantage of the extra cores. This move towards parallel processing has been complicated by the diversity and heterogeneity of the various parallel architectures that are now available. A heterogeneous system is made up of different processors each with specialized capabilities. Over the last several years, GPUs have been targeted as yet another source of computing power in the system.

GPUs, which have always been very parallel—counting hundreds of parallel execution units on a single die—have now become increasingly programmable, to the point that it is now often useful to think of GPUs as many-core processors instead of special purpose accelerators.

All of this diversity has been reflected in a wide array of tools and programming models required for programming these architectures. This has created a dilemma for developers. In order to write highperformance code they have had to write their code specifically for a particular architecture and give up the flexibility of being able to run on different platforms. In order for programs to take advantage of increases in parallel processing power, however, they must be written in a scalable fashion. Developers need the ability to write code that can be run on a wide range of systems without having to rewrite everything for each system.

OpenCL[™] for Unified, Portable Source Code

OpenCL[™], the first open and royaltyfree programming standard for generalpurpose parallel computations on heterogeneous systems, is quickly growing in popularity as a means for developers to preserve their expensive source code investments and easily target multi-core CPUs and GPUs.

OpenCL is maintained by the Khronos Group, a not-for-profit industry consortium that creates open standards for the authoring and acceleration of parallel computing, graphics, dynamic media, computer vision and sensor processing on a wide variety of platforms and devices. Developed in an open standards committee with representatives from major industry vendors, OpenCL affords users a cross-vendor, non-proprietary solution for accelerating their applications across mainstream processing platforms, and provides the means to tackle major development challenges, such as maximizing parallel compute utilization, efficiently handling data movement and minimizing dependencies across cores.

Ultimately, OpenCL enables developers to focus on applications, not just chip architectures, via a single, portable source code base. When using OpenCL, developers can use a unified tool chain and language to target all of the parallel processors currently in use. This is done by presenting the developer with an abstract platform model that conceptualizes all of these architectures in a similar way, as well as an execution model supporting data and task parallelism across heterogeneous architectures.

Key Concepts and Workflows

OpenCL has a flexible execution model that incorporates both task and data parallelism. Tasks themselves are comprised of data-parallel kernels, which apply a single function over a range of data elements in parallel. Data movements between the host and compute devices, as well as OpenCL tasks, are coordinated via command queues.

An OpenCL command queue is created by the developer through an API call, and associated with a specific compute device. To execute a kernel, the kernel is pushed onto a particular command queue. Enqueueing a kernel can be done asynchronously, so that the host program may enqueue many different kernels without waiting for any of them to complete. When enqueueing a kernel, the developer optionally specifies a list of events that must occur before the kernel executes. If a developer wishes to target multiple OpenCL compute devices simultaneously, the developer would create multiple command queues.

Command queues provide a general way of specifying relationships between tasks, ensuring that tasks are executed in an order that satisfies the natural dependencies in the computation. The OpenCL runtime is free to execute tasks in parallel if their dependencies are satisfied, which provides a general-purpose task parallel execution model.

Events are generated by kernel completion, as well as memory read, write, and copy commands. This allows the developer to specify a dependence graph between kernel executions and memory transfers in a particular command queue or between command queues themselves, which the OpenCL runtime will traverse during execution. Figure 1 shows a task graph illustrating the power of this approach, where arrows indicate dependencies between tasks. For example, Kernel A will not execute until Write A and Write B have finished, and Kernel D will not execute until Kernel B and Kernel C have finished.

The ability to construct arbitrary task graphs is a powerful way of constructing taskparallel applications. The OpenCL runtime has the freedom to execute the task graph in parallel, as long as it respects the dependencies encoded in the task graph. Task graphs are general enough to represent the kinds of parallelism useful across the spectrum of hardware architectures, from CPUs to GPUs.

Besides the task parallel constructs provided in OpenCL, which allow synchronization and communication between kernels, OpenCL supports local barrier synchronizations within a work-group. This mechanism allows work-items to coordinate and share data in the local memory space using only very lightweight and efficient barriers. Workitems in different work-groups should never



Command Queue.

try to synchronize or share data, since the runtime provides no guarantee that all workitems are concurrently executing, and such synchronization easily introduces deadlocks.

Developers are also free to construct multiple command queues, either for parallelizing an application across multiple compute devices, or for expressing more parallelism via completely independent streams of computation. OpenCL's ability to use both data and task parallelism simultaneously is a great benefit to parallel application developers, regardless of their intended hardware target.

Kernels

As mentioned, OpenCL kernels provide data parallelism. The kernel execution model is based on a hierarchical abstraction of the computation being performed. OpenCL kernels are executed over an index space, which can be 1, 2 or 3 dimensional. In Figure 2, we see an example of a 2 dimensional index space, which has Gx * Gy elements. For every element of the kernel index space, a work-item will be executed. All work items execute the same program, although their execution may differ due to branching based on data characteristics or the index assigned to each work-item.

The index space is regularly subdivided into work-groups, which are tilings of the entire index space. In Figure 2, we see a work-group of size Sx * Sy elements. Each work-item in the work-group receives a work-group id, labeled (wx, wy) in the figure, as well as a local id, labeled (sx, sy) in the figure. Each work-item also receives a global id, which can be derived from its work-group and local ids.

Work-items in different work-groups may coordinate execution through the use of atomic memory transactions, which are an OpenCL extension supported by some OpenCL runtimes. For example, work-items may append variable numbers of results to a shared queue in global memory. However, it is good practice that work-items do not, generally, attempt to communicate directly, as without careful design scalability and deadlock they can become difficult problems. The hierarchy of synchronization and communication





AMD EMBEDOED SOLUTIONS

> provided by OpenCL is a good fit for many of today's parallel architectures, while still providing developers the ability to write efficient code, even for parallel computations with non-trivial synchronization and communication patterns.

The work-items may only communicate and synchronize locally, within a work-group, via a barrier mechanism. This provides scalability, traditionally the bane of parallel programming. Because communication and synchronization at the finest granularity is restricted in scope, the OpenCL runtime has great freedom in how work-items are scheduled and executed.

A Typical OpenCL Kernel

As already discussed, the core programming goal of OpenCL is to provide programmers with a data-parallel execution model. In practical terms this means that programmers can define a set of instructions that will be executed on a large number of data items at the same time. The most obvious example is to replace loops with functions (kernels) executing at each point in a problem domain.

Referring to Figures 3 and 4, let's say you wanted to process a 1024×1024 image (your global problem dimension). You would initiate one kernel execution per pixel ($1024 \times 1024 = 1,048,576$ kernel executions).

Figure 3 shows sample scalar code for processing an image. If you were writing very simple C code you would write a simple for loop, and in this for loop you would go from 1 to N and then perform your computation.

An alternate way to do this would be in a data parallel fashion (Figure 4), and in this case you're going to logically read one element in parallel from all of a (*a), multiply it from an element of b in parallel and write it to your output. You'll notice that in Figure 4 there is no for loop—you get an id value, read a value from a, multiply by a value from b and then write the output.

As stated above, a properly written OpenCL application will operate correctly on a wide range of systems. While this is true it should be noted that each system and compute device available to OpenCL may have different resources and characteristics that allow and sometimes require some level of tuning to achieve optimal performance.

FIGURE 3	Example of traditional loop
	(scalar).

```
kernel void
dp_mul (global const float *a,
            global const float *b,
            global float *c)
{
    int id = get_global_id (0);
    c[id] = a[id] * b[id];
} // execute over "n" work-items
```

FIGURE 4 Data parallel OpenCL.

For example, OpenCL memory object types and sizes can impact performance. In most cases key parameters can be gathered from the OpenCL runtime to tune the operation of the application. In addition, each vendor may choose to provide extensions that provide for more options to tune your application. In most cases these are parameters used with the OpenCL API and should not require extensive rewrite of the algorithms.

Building an OpenCL Application

An OpenCL application is built by first querying the runtime to determine which platforms are present. There can be any number of different OpenCL implementations installed on a single system. The desired OpenCL platform can be selected by matching the platform vendor string to the desired vendor name, such as "Advanced Micro Devices, Inc." The next step is to create a context. An OpenCL context has associated with it a number of compute devices (for example, CPU or GPU devices). Within a context, OpenCL guarantees a relaxed consistency between these devices. This means that memory objects, such as buffers or images, are allocated per context; but changes made by one device are only guaranteed to be visible by another device at well-defined synchronization points. For this, OpenCL provides events, with the ability to synchronize on a given event to enforce the correct order of execution.

Most OpenCL programs follow the same pattern. Given a specific platform, select a device or devices to create a context, allocate memory, create device-specific command queues, and perform data transfers and computations. Generally, the platform is the gateway to accessing specific devices. Given these devices and a corresponding context, the application is independent of the platform. Given a context, the application can:

- Create one or more command queues.
- Create programs to run on one or more associated devices.
- Create kernels within those programs.
- Allocate memory buffers or images, either on the host or on the device(s)
 Memory can be copied between the host and device.
- Write data to the device.
- Submit the kernel (with appropriate arguments) to the command queue for execution.
- Read data back to the host from the device.

The relationship between context(s), device(s), buffer(s), program(s), kernel(s), and command queue(s) is best seen by looking at sample code.

Summary

OpenCL affords developers an elegant, non-proprietary programming platform to accelerate parallel processing performance for compute-intensive applications. With the ability to develop and maintain a single source code base that can be applied to CPUs, GPUs and APUs with equal ease, developers can achieve significant programming efficiency gains, reduce development costs, and speed their time to market.

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Model	x86 Core Clock Speed Base/ Boost	L2 Cache	GPU	DDR3 Speed	x86 Cores	UVD ¹ 3	Display Ouptuts	Max TDP	
AMD Embedded G-Series APU - F11 413-pin									
T56N	1.65GHz		AMD Radeon™ HD 6320		2			18W	
T56E	1.65GHz		AMD Radeon™ HD 6250	DDR3-1333 Unbuffered	2	_	Dual independent display controllers 2 active outputs from: 1xVGA 2x single link DVI 1X single link LVDS 2x DisplayPort 1.1a 1x HDMI	18W	
			AMD Radeon™ HD 6310		1			18W	
T52R	1.5GHz		AMD Radeon™ HD 6250	250 DDR3-1066 Unbuffered		1		18W	
T48E	1.4GHz				2	Yes			
T44R	1.2GHz		AMD Radeon™ HD 6250	DDR3-10663	1			9W	
T40N	1.0GHz ³		AMD Radeon™ HD 6290	Unbuffered	2			9W	
T48n	1.4GHz	512KB	AMD Radeon™ HD 6310	DDR3-1066 Unbuffered	2			18W	
T40E	1.0GHz		AMD Radeon™ HD 6250	DDR3-10663	2		1X DVO	6.4W	
T40R	1.0GHz		AMD Radeon™ HD 6250	Unbuffered	1			5.5W	
T16R	615mHz		AMD Radeon™ HD 6250	LVDDR3-1066	1			4.5W	
T48L	1.4GHz		N/A	DDR3-1066	2			18W	
T30L	1.4GHz		N/A	Unbuffered	1		NVA	18W	
T24L	1.0GHz		N/A	DDR3-1066 ³ Unbuffered	1	N/A	N/A	5W	

1. Unified Video Decoder (UVD 3) for hardware decode of high-definition video.

2. Low voltage (1.35V) DDR3 is assumed for the 9W TDP processors. The use of 1.5V DDR3 will incur a power adder.

3. Models enabled by AMD Turbo CORE technology, up to 10% clock speed increase is planned. For CPU boost, only one processor core of a dualcore has boost enabled.

Note: Always refer to the processor/chipset data sheets for technical specifications. Feature information in this document is provided for reference only.





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AMD APUs Soar in Real-Time Image Processing

hen the Company for Advanced Supercomputing Solutions (CASS) was approached by an Israeli defense contractor to create a new field video image registration solution, it was their first venture in working with an AMD Embedded accelerated processor unit (APU). It won't be the last.

The defense contractor's executives had come to CASS with a problem: they needed high-quality, smooth, stable real-time computer vision images delivered from ground and aero systems to back-end systems. The defense contractor's digital signal processing (DSP) and field-programmable gate array (FPGA) solutions were not capable of developing the high-speed, higher-resolution images that could more accurately track motion—tracking missiles as they are carried on a moving vehicle or detecting a person climbing into a bunker, for example.

CASS was asked to create a compact system that could process a frame-by-frame 720p video input stream at 120 frames per second. While the defense contractor imposed constraints around maximum size and maximum power consumption, CASS was otherwise unlimited in how it could design the solution.

So, the company got creative. By making the right algorithmic adjustments and choosing an appropriate architecture, the resulting application runs at real-time speeds where other competitive solutions (DSP and FPGA) failed to meet the requirements. The resulting solution built by CASS can serve as a new-generation DSP for sensor and computer-vision platforms, leveraging a combination of parallel and serial processing on a heterogeneous system architecture.

The challenge

"Lots of industries use graphics processing units (GPUs) for projects that include video," said Mordechai "Moti" Butrashvily, CASS chief executive officer and chief technology officer. CASS has been building solutions around AMD GPUs for years and knew that for applications with a high-degree of parallelism—like image processing —programmable GPUs offer critical performance advantages. "But we knew a stand-alone GPU just couldn't offer a solution that would meet the power consumption and size constraints of the defense contractor."

Butrashvily and his team looked at a variety of possible solutions, and realized their options were rather limited. Few manufacturers can offer the performance needed without compromising on size or power consumption. The CASS team found their research kept pointing them to the AMD Embedded G-Series APU, which combines the parallel processing capabilities of a GPU with the serial processing capabilities of a CPU in a small footprint and low power solution.

"We evaluated several solutions, and nothing else compared to the APU for size, power consumption and capabilities. No one else provides a similar solution in terms of performance per watt" Butrashvily said. "One additional advantage of the AMD G-Series APU is that they are sold as embedded solutions, meaning a good fit for defense solutions that require long-term availability and durability in harsh environments."

Real-Time Threat Detection

"[The defense contractor] needed semiautomatic systems that could help aid pilots in making decisions" explained Butrashvily. "The way to do that is to take images from both aerial and ground systems to stabilize video streams, enabling the detection of immediate threats." They required a sys-

Image Registration

Image registration is the process of transforming a set of sequential images (video stream acquired from a sensor) into a similar coordinate system, creating a smoother visual flow. In real-life, physical conditions or normal movement affect the images a sensor gathers and may cause vibrations.

Viewing a continuous frame-set from an image sensor generally looks shaky or unbalanced, as the sensor is often mobile or not stabilized. Image registration fixes this problem by smoothing the output video stream. Applications for image registration vary from defense to medical imaging and more.

Typical registration process stages include: identifying movement vectors between two relative images, performing alignment, and applying further correction/enhancement filters to improve image and stream quality.

In defense, sensor-based components use registration from ground to aerial systems with different applications. Adding to its complexity, defense applications require very high performance computations (high resolutions and frame rates) and have limited space for hardware, dictating a small system size. This requires a solution with good heat dissipation and ability to consistently operate at low power. tem that was compact and low power enough to be used in unmanned aerial and ground vehicle (UAV and UGV) surround-vision systems for continuous monitoring of objects and threats anywhere in the world.

AMD

The AMD G-T56N APU met the power requirements of the system, and could deliver the high performance necessary to meet the image registration goals. Since the processor had to employ further image filtering to enhance results, CASS needed to ensure there was enough performance overhead to run additional algorithms while maintaining real-time operation. CASS selected OpenCLTM to implement the accelerated algorithm building blocks.

In the prototype the APU served as a digital signal and image processor, and was connected to a sensor. "We tested the APU to see if we could achieve the realtime performance the sensors require," Butrashvily explained. "There was no option for delays: the signal had to be processed at the time it was being received with minimum latency."

The entire algorithm was implemented in OpenCL, with the APU serving as the host manager/coordinator and frame grabber. With the goal to achieve

faster-than-real-time processing, CASS leveraged parallel processing for the intensive dense matrix operations, including GEMM (matrix multiplication), GEMV (matrix-vector multiplication) and GESV (matrix Inverse), achieving up to 130 times the performance of running those basic building blocks with the AMD BLAS (basic linear algebra subprograms) libraries on the processor alone. To verify the numeric stability, which is especially important in longrunning, mission-critical operations, the arithmetic results of the APU were compared to the x86 CPU following IEEE 754 standard. CASS found high correspondence and accuracy, assuring that the system achieves great numerical stability.

The Results

Within two months, CASS completed the prototype development, including software optimization. The solution was developed to support Linux, Windows and their embedded variants. The algorithmic processing engine was also integrated with OpenGL, delivering a live display of the processed results. "The AMD G-T56N APU de-

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livered very well for the selected application and environment," Butrashvily explained. "This solution provides unmatched performance when you take into account the power consumption and size requirements."

The performance achieved was impressive; showing nearly 150 frames per second (FPS) peak at HD resolution of 1280x720 with 16-bits per pixel, measured from input to output of corrected images. With the AMD Embedded G-Series APU, CASS was able to achieve the following:

- Real-time performance
- Processing of 120 frames per second sustained
- HD sensor input resolution of 720p (1280x720)
- 20 to 30 times the performance of performing the entire algorithm on a traditional CPU

The overall algorithm processing flow was complex, incorporating additional filters for image enhancement, therefore runtime speedup was summarized by 20 to 30 times.

For its next steps, CASS is working on support for hard real-time operating systems, hardware commercialization and board design to match sensor dimensional constraints, and support for next-generation APUs for even higher performance and resolutions.

Moreover, because the job was not proprietary to the defense company, CASS is researching additional applications of its new APU-based image registration technology. Being an important core component in many image-processing systems, registration has relevance for other applications in defense, medical imaging and machine vision.





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Android Goes Beyond Google

Android is finding uses in more than just the mobile market. The coming expansion further into these markets will involve opportunities and risks and require resources beyond the intentions of Google.

by Art Lee, Viosoft

s of Ice Cream Sandwich (ICS), Android as delivered by Google is a software platform largely targeted at the mobile handset and tablet market. The Google Android software development environment and programming interfaces (APIs) are geared toward enabling applications written for this market. For the non-mobile market, the challenges and opportunities begin with the breakaway intent to repurpose the Android platform for any consumer product that requires a touch-oriented user interface, high-performance multimedia recording and playback, and/or application portability. We will look at some of the challenges associated with these product scenarios as well as examine a case study of an approach developed by Viosoft to assist OEMs in this task.

Portability versus Performance

Applications written for traditional embedded devices are specific to the underlying hardware architecture and OS that host the platforms. In many cases, embedded applications need to be rewritten, or ported to a specific platform. This process, referred to as "re-targeting," can significantly add to the costs of the development and testing of embedded software.

This is where the appeal of the Android platform's application portability comes in. The concept of "write once, run many" suggests that the same application binaries, written for and tested on one Android platform of a given architecture, shall



FIGURE 1 Android Architecture diagram.



FIGURE 2 Integration Framework for Android.

run identically on another Android platform of a different architecture. This is not a new concept but rather one that existed when James Gosling of (now defunct) Sun Microsystems gave birth to the Java programming language more than a decade ago. The generally interpretive nature of the language means that Java applications tend to run slower than those for compiled languages (C/C++).

Android leverages Java, but not entirely. To better understand this, let's look more carefully at the Android Software stack (Figure 1). Android applications (in blue) are written in Java, but they rely on the application framework, associated libraries and runtime consisting of over fifteen million lines of some Java and mostly C/C++ code. The partition between Java and C/C++ language in the Android design is premised on performance, with "slower" code on the Java side, and "faster" code on the C/C++ side. Under this framework, the developer is presented with the option to 1) write a pure Java application that relies exclusively on the pre-established C/C++ "sandbox" for acceleration and achieve 100% portability, or 2) write a self-containing C/C++ application wrapped in Java that is specific to a given architecture. Given the current state of near homogeneity of Android around the ARM architecture, and the success of vendors like Rovio (Angry Bird) who have taken the latter approach, the Android developer market has spoken in favor of performance.

Recent releases of Android have added a Hardware Abstraction Layer (HAL) to address the needs of high-performance native applications. The Android HAL wraps the Linux kernel drivers to create a layer of abstraction for native applications to access location (GPS), Wi-Fi, 2D/3D graphics, audio/video and other hardware specific to a mobile use profile. While the Android HAL has helped to simplify hardware integration for OEMs and device manufacturers, it's not clear how the HAL delineates from the abstraction of the Linux kernel itself, or how it will evolve to incorporate non-mobile use cases.

Android, in Embedded and beyond Google

In advocating the adoption of "Android beyond Google," we envisage Android being ported for and integrated into products that do not meet the mobile use profile of smartphones or tablets, or necessarily use a CPU powered by the ARM architecture. Yet, these products still require and benefit from the touch GUI, application portability and multimedia capabilities and resources that Android provides. Printers, digital camcorders, set-top boxes and smart TVs are just a few examples of how Android can potentially be used outside of mobile.

One of the primary challenges in repurposing Android is the ability for applications to (inter) operate in and out of the Android runtime sandbox. Just as with Linux applications, native (C/C++)Android code often needs to access runtime libraries for string or math operations. On standard Linux desktops, these operations are provided as part of the GNU runtime environment (i.e., glibc and libm). For performance and footprint reasons, these are supplanted by the Bionic libraries in the Android runtime environment. While both Bionic and the GNU libraries are largely semantically and syntactically equivalent, they are not runtime compatible. This means that Linux application binaries cannot run in the Android sandbox, and vice versa. A second challenge adds to this incompatibility divide: most, if not all Linux applications have a graphical interface that relies on X11, whereas Android applications rely on the Android framework and HAL to render graphics. OEMs and developers must develop approaches to reconcile between Bionic and GNU libraries, and between X11 and the Android frame-buffer, as part of the strategy to benefit from embedding Android.

Integration Framework for Android

One such approach to reconcile between Android and legacy Linux applications is Viosoft's Integration Framework for Android. Under this framework, applications are deployed under two separate containers—one hosting Android and the other X11-based Linux applications. Applications in the Linux container can be launched and controlled by



the Android desktop, while maintaining full compatibility with existing legacy libraries and drivers. Figure 2 shows a high-level architectural diagram of the framework.

To verify the viability of this approach, we've implemented a full media center for Android on the AMD G-Series STB reference board. Before diving into the implementation details, let's have a look at the hardware. The G-Series family combines two 64-bit x86 processors with a Graphics Processing Unit (GPU) that consists of 80 floating point engines. The STB reference platform that we used is clocked at 1.6 GHz, equipped with full HDMI /Component out, wireless and 10/100 Ethernet, 2 Gbyte of memory and a 320 Gbyte SATA drive. Utilizing the Integration Framework for Android, we were able to deploy a full port of Android 4.0 ICS, running simultaneously with other legacy Linux applications such as XBMC (Xbox Media Center) and the Open Office Suite.

Porting Android to the G-Seriesbased STB was straightforward. Most of the code pulled from the Android for x86 projects (http://www.android-x86. org/) built and ran out of the box, albeit at VESA resolution. Nonetheless, this baseline enables us to leverage all of the applicable resources of Android.

Our next step was to fine tune a variety of kernel drivers to take full advantage of the hardware capabilities of the STB, including full 1080p streaming/playback and networking support for both wired and wireless interfaces. Once this work was completed, we examined the X11 requirement by XBMC and Open Office and ensured that both the X11 server and Android graphics subsystem could share audio and video resources while executing out of two separate runtime containers. The Integration Framework for Android fundamentally acts as a bridge between the Android Application Framework and native Linux applications.

As shown in Figure 3, icons are displayed in the Android Desktop for both XBMC and Open Office (circled in red). These icons are used to launch the respective applications, putting the Android



FIGURE 3 Android 4.0 desktop with native application icons (circled in red).

desktop in the background. The launched application then has direct and full access to the underlying resources necessary to render graphics and audio/video contents. At the same time, other Android services will continue to respond to stimuli in the background, and if necessary, relinquish control of the display to solicit input from the user. For example, an incoming Skype call would interrupt an XMBC movie playback, giving the user the option to pick up the call.

The end result is a surprisingly fluid and functional media experience, hosted by the modern look and feel of the Android front-end, while at the same time being fully capable of tapping into the large body of stable and functionally rich desktop Linux applications. The same environment can readily power a variety of real-world applications such as touch-based medical equipment products and user consoles for industrial control.

An exciting aspect of this work is in the potential to repurpose Android toward different use profiles that have needs for Android and native Linux application interoperability. The ability to reuse existing code while benefiting from some of Android's modern capabilities can result in significant costs and time savings to OEMs.

An essential challenge often presented to developers by multi-faceted environments like the Integration Framework is the lack of debug visibility for application logic that straddles runtime or language boundaries. When a function call crosses over from Java into C/ C++, developers are often at a loss in their ability to follow through the flow in the process of tracking down a program defect-making a multi-lingual debug environment an indispensable tool for such needs. Arriba for Android is the only tool of its kind to fully integrate mixed language, multicore and multidomain debugging for Android and Linux applications into a single environment. Arriba's "run mode" debug feature yields complete transparency to all layers of the Androidbased platform, making it practical for the developer to visualize the flow of the system in its entirety.

With this level of visibility and control, Arriba can dramatically reduce development time and costs associated with product development. Bundled with the Integration Framework for Android, Arriba offers the OEM a complete environment to rapidly develop and deploy Androidenabled products with higher reliability and significantly lower costs.

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MICPUTER Mini-ITX Single Board 微空習能 Computer AF2X624 AF2X62A

- AMD Embedded G-T56N APU with AMD Radeon[™] HD 6320 Graphics
- 1 * SO DIMM DDR3 800/1333MHz of memory up to 4GB • Realtek ALC883, support 2/4/5.1/7.1 HD
- sound channel
- 1* Realtek 8111C,10/100/1000M, support PXE boot
- 8 x USB 2.0,2 x UART,2 x MINI_PCIe,4 x SATA,1 x SPDIF,2 x PS-S EL (SATA and PCIE header
- 1 x HDMI,2 x VGA,1 x RJ45,1 x AUDIO,4 x USB • Mini-ITX 170*170mm, DC Power 12~24
- VDC/5A (Optional)

SHENZHEN XINZHIXIN ENTERPRISE DEVELOPMENT CO., LTD

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MICPUTER 微控智能

Nano-ITX Single **Board Computer** NANO-AF2S1A/E

- AMD Embedded G-Series Platform
- OS Supported: Linux[™], Windows[™] 7
- Power Consumption: <25W
- Memory: SODIMM, up to 4GB, DDR3, 1x 1333/1066/800
- Industrial Controllers, Digital Set Top Boxes, Digital Signage, Point-of-Sale, Thin Clients

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• Exceptional graphics performance (up to 576 GFLOPs), enabling reliable and low power applications with amazing user experiences and smooth, vivid HD video.

AMD EMBEDDED SOLUTIONS R-SERIES APU

- Supports AMD Radeon[™] Dual Graphics technology¹ for more than double graphics performance compared to using discrete graphics alone.
- Innovative CPU architecture integrates dedicated resources that deliver exceptional performance, with shared resources that reduce power consumption and die space.

HOWTIMES

EMBEDDED SOLUTIONS

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- Drive up to 4 displays² directly or up to 10 independent displays by pairing an AMD R-Series APU with an AMD Radeon[™] Embedded discrete graphics processor or card.
- Supports a wide range of parallel compute capabilities to suit the requirements of many embedded applications.

